FDP on VLSI Testing and Testability (14th July- 20th July 2025)

	9-10 AM	10-11 AM	11-12 PM	12-1 PM	1-6 PM	6-7 PM	7-8 PM	Hours(40)
Monday; 14th July, 2025	Introduction to VLSI Testing		Types of Faults, Fault collapsing			Introduction to Semiconductor Chips' testing		
	Prof. Virendra Singh		Dr. Menka Yadav			Prof. CP Ravikumar		
	IIT Bombay		MNIT Jaipur			Vinyana Tech.		6
Tuesday; 15th July, 2025	Memory Testing		Fault Simulation, Combinational Testing- Boolean difference, SCOAP			D-algo, PODEM	Reliability	
	Prof. Virendra Singh		Dr. Menka Yadav			Dr. Menka Yadav	r. Harsahay Jaiswar	
	IIT Bombay		MNIT Jaipur			MNIT Jaipur	OSRAM, Astria	6
Wednesday; 16th July, 2025	for Single-Clock Synchronous C		Test pattern Generation Techniques I			Scan Test Illustration		
	Prof. Virendra Singh		Dr. Menka Yadav			Prof. CP Ravikumar		
	IIT Bombay		MNIT Jaipur			Vinyana Tech.		6
Thursday; 17th July, 2025						Logic BIST		
	Sequential circuits- aliasing and its effect on fault coverage.		Test pattern Generation Techniques II			Prof. CP Ravikumar		Quiz 1
	Prof. Virendra Singh		Dr. Menka Yadav			Vinyana Tech.		5
	IIT Bombay		MNIT Jaipur					
Friday; 18th July, 2025			VLSI Testing Advances					
	Test compression, signature an		Mr. Tarun Goyal			Memory BIST		
	Vineet Sahula		NXP Semiconductors			Prof. CP Ravikumar		
	MNIT Jaipur					VInyana Tech.		6
Saturday; 19th July, 2025								
	Combinational & sequential equivalence		VLSI Testing Advances			Analog Test and Boundary Scan		
	Vineet Sahula		Mr. Deepak Agrawal			Prof. CP Ravikumar		Quiz2
			HrdWyr Pvt. Limt. Bangalore			Vinyana Tech.		6
Sunday; 20th July, 2025			SoC Verification			Low Power Test and Reliability Test		
	Latest trends in VLSI and how AI is shaping Semiconductor growth		Ir. Prateek Mudgil			Prof. CP Ravikumar		
	Mr. Surendra Tadi		Synopsis, Noida			Vinyana Tech.		
	Qualcomm WLAN, Bangaluru				Break			5