MALAVIYA NATIONAL INSTITUTE OF TECHNOLOGY JAIPUR
JLN MARG, JAIPUR-302 017 (RAJASTHAN) INDIA

Prof. I.K. Bhat
Director

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23rd Nov. 2015

Mr. Sanjiv Mittal IAS
Jt. Secretary
Dept. of Electronics & Information Technology
Electronics Niketan, 6-CGO Complex, Lodhi RoadNew Delhi – 110 003
Phone: 011- 24363075; Fax- 011- 24363099, Email- sanjiv.mittal@deity.gov.in

Sub: Letter from Mr. P Victor Albuquerque; Letter no. 3(6)2012-HRD (Vol-V) dated 18-Nov-2015

Ref: (i) Signing of MoU under "Scheme for financial assistance for setting up Electronics &ICT Academies" proposal from MNIT Jaipur (Category-B)&(ii) CI/Co-CIs/Academic Persons nomination

Dear Sir

We thank you for informing us about approval of Electronics &ICT Academy (Category-B) to our institute. We have already consented for the same, and now forwarding the signed Memorandum of Understanding (MoU). It will be our endevour to come up to your expectations and fulfill the onjectives for which the academy is to be set up.

The following would be Chief coordinator/Co-CI/Academy-Chairperson at MNIT Jaipur for the academy.

(i).	Mentor Institute :	**Malaviya National Institute of Technology Jaipur**
(ii).	States to which Catering:	Rajasthan, Gujarat, Dadra & Nagar Haveli, Daman & Diu
(iii).	Chief Investigator	NAME : Prof. Vineet Sahula Email :vsahula.ece@mnit.ac.in; Mobile No. :954 9654 227
(iv).	Co- Chief Investigators	NAME :Dr. L. Bhargava, PhD Email: lavab@mnit.ac.in; Phone: 954 9654 231 NAME :Dr. S. J. Nanda, PhD Email: sjnanda.ece@mnit.ac.in;Phone: 954 9654 237 NAME :Dr. C. Periasamy, PhD Email: cpsamy.ece@mnit.ac.in; Phone: 954 9654 235 NAME :Dr. Emanual S. Pilli, PhD Email: espilli.cse@mnit.ac.in;Phone: 954 9658 131 NAME :Head, Dept of ECE, Ex-officio (currently Prof. K. K. Sharma) Email: hod.ece@mnit.ac.in; Phone: 954 9658 228 NAME :Head, Dept. of CSE, Ex-officio (Currently Prof. M. C. Govil), Email: hod.cse@mnit.ac.in; Phone: 954 9658 134

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(v) Chairperson of Academy: Name : Prof. V. Sinha (Prof. Emeritus MNIT Jaipur)
Email: vsinha@iitk.ac.in; mobile: 94140 76634

(vi) Director of the Institute NAME : Prof. I. K. Bhat
Email :ikbhat@mnit.ac.in
Mobile No./ Contact No. :954 9373 000

(vi). Area of Specialization: Embedded Systems design & security; computer networking & security, nano-electronic devices & circuits; soft-computing & data mining;

(vii) For more details: (webpage address) * : www.mnit.ac.in

With kind regards

Yours Sincerely

(I. K. Bhat)

Copy: Mr. Victor Albuquerque
Deputy Director, Dept. of Electronics & Information Technology
Electronics Niketan, 6-CGO Complex, Lodhi Road New Delhi – 110 003
Phone: 011- 24301394; Fax- 011- 24366558-59, Email- p.victor@nic.in

MEMORANDUM OF UNDERSTANDING

This Memorandum of Understanding (MOU) is made on 23rd NOV. 2015 2015 between:

a) **The President of India** acting through the Department of Electronics and Information Technology, Ministry of Communications and Information Technology, Electronics Niketan, 6, CGO Complex, New Delhi-110003. (hereinafter referred to as DeitY, which expression shall, unless excluded by or repugnant to the context, be deemed to include his successors in office and assigns) of the FIRST PART;

AND

b) **Malaviya National Institute of Technology, Jaipur** (hereinafter referred to as **Implementing Agency,** which expression shall, unless excluded by or repugnant to the context, be deemed to include his successors in office and assigns) of the SECOND PART.

WHEREAS DeitY has sponsored a scheme entitled '***Scheme for Financial Assistance for setting up of Electronics and ICT Academies'*** (hereinafter referred to as the Electronics and ICT Academy Scheme) under the Plan Scheme viz. 'Digital India and Manpower Development', under which Seven (07) Electronics & ICT Academies in two Categories (A & B) are to be set up in the country, as a unit in existing institutions for faculty/mentor development/upgradation to improve the employability of the graduates/diploma holders in various streams. Under this scheme, each selected institute would set up an Electronics and ICT Academy in a project mode which will be funded by Government of India for a period of four (04) years. In the instant case the Implementing Agency has been selected to set up a Category **B** Academy.

NOW THEREFORE in consideration of the premises and mutual covenants hereinafter contained, the parties hereto agree as follows:

1. DEFINITIONS

Unless otherwise stated, for the purpose of this MOU, the terms given hereunder shall have the following meanings:

(i) **Annexure**: Any annexure to this MOU as enumerated and cross-referred in these articles.
(ii) **Articles**: Any Clause of this MOU or partial clause with separate marginal number as referred to anywhere in the workings of this MoU or its Annexures.
(iii) **DeitY**: Department of Electronics and Information Technology, Government of India having its office at 6, CGO Complex, New Delhi - 110003.
(iv) **GIA**: Grants-in-Aid.
(v) **IA**: Implementing Agency
(vi) **IPR**: Shall mean all rights, benefits, title or interest in or to any Intellectual Property (whether registered or not and including all applications for the same).
(vii) **IR:** Internal Revenue.
(viii) **Party/Parties** means DeitY or/and **Implementing Agency**
(ix) **Scheme:** Scheme for Financial Assistance for setting up of Electronics and ICT Academies.

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(x) **Project**: Setting up of Electronics and ICT Academy by a selected institute with financial support from Government of India for a period of four (04) years.

2. SCOPE OF MEMORANDUM OF UNDERSTANDING

The Articles 1 to 18 and Annexure I to III to this MOU form an integral part of the MOU between the parties. The terms herein referred in the MOU and Annexures shall be binding on the parties. The MOU together with the Annexures indicates the responsibilities and obligations of the parties to this MOU including terms and conditions, financial arrangement, intellectual property rights, monitoring mechanism etc. of the Project.

3. AREA OF COVERAGE / TRAINING TARGET

(a) The faculty of various academic institutions cutting across engineering / arts / commerce / science colleges / polytechnics across the country would be covered.

(b) Training Target is as follows:

Category	Target for 4 years per Academy	Number of Academies	Total target
A	16,000	05	80,000
B	6,400	02	12,800
Total		**07**	**92,800**

4. IMPLEMENTATION STRUCTURE OF THE PROJECT

4.1 The implementation of the scheme would be carried out through the following:

(a) Each Electronics & ICT academies would cater to a particular region. The regional distribution of States/UTs among the selected States and indicative states/UTs to be catered to by each Academy as under:

S. No.	Region	Approved/Recommended State / Institution	Indicative States/UTs to be catered (alphabetically)
1	Eastern	**Bihar**: NIT-Patna (**Category A**)	Bihar, Jharkhand, Odisha, West Bengal
2	Western/Central	**Madhya Pradesh**: IIITD&M-Jabalpur (**Category A**)	Chattisgarh, Madhya Pradesh, Maharashtra
3		**Rajasthan :** MNIT-Jaipur (**Category B**)	Gujarat, Rajasthan, Dadra & Nagar Haveli, Daman & Diu
4	Northern	**Uttar Pradesh:** IIT-Kanpur (**Category A**)	Delhi, Chandigarh, Haryana, Punjab, Uttar Pradesh
5		**Uttarakhand:** IIT-Roorkee (**Category B**)	Jammu & Kashmir, Himachal Pradesh, Uttarakhand
6	North Eastern	**Assam**: IIT-Guwahati (**Category A**)	Assam, Arunachal Pradesh, Manipur, Meghalaya, Mizoram, Nagaland, Tripura, Sikkim
7	**Southern [ICT Academy set-up in the states of Tamil Nadu and Kerala]**	**Telangana**: NIT-Warangal (**Category A**)	Andhra Pradesh, Karnataka, Puducherry, Andaman and Nicobar Island, Telangana, Goa
		***Kerala:** ICT Academy-Kerala	Kerala, Lakshadweep,
		***Tamil Nadu :** ICT Academy-Tamil Nadu	Tamil Nadu
	* No funding is envisaged to Kerala & Tamil Nadu ICT Academies under the instant scheme as these Academies were/are separately funded by DeitY.		

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(b) The representatives of all the States in a particular region would be included under the Advisory Board to be created by each Academy, which could oversee the implementation of the Academy and ensure that faculty of all these States are appropriately covered.

(c) The Scheme for setting up the Electronics and ICT Academy would be in operation for five (05) years. Each Electronics and ICT Academy would be provided financial support for four (04) years in a project mode as per their Category.

(d) A Project Management Unit (PMU) has been set up by National Institute of Electronics & Information Technology (NIELIT) for implementation and management of various activities under the project.

(e) The detailed guidelines on common operational and functional framework for all the Academies would be as issued by DeitY. Each selected institution/Academy would need to abide by these guidelines.

5. RESPONSIBILITIES OF DeitY & Implementing Agency

5.1 Responsibilities of DeitY

(i) To set up and organize meetings of the Empowered Committee for taking policy level decisions, select the institutions, operational structure, etc.

(ii) To ensure time-bound implementation of the Scheme / Project, set up and organize meetings (from time to time) of Project Review and Steering Group (PRSG).

(iii) To provide necessary funds for the implementation to the respective Institutions based on recommendation of the Empowered Committee (for first installment of grants-in-aid) and Project Review and Steering Group (for second installment onwards), and/or assessment by DeitY and as approved by DeitY.

(iv) To assist in expediting issues related to the progress of this Scheme / Project, coordination with the relevant Govt. departments/ organisations/ institutions and other agencies concerned.

(v) To take up any other issues and aspects related to the Scheme / Project.

5.2 Responsibilities of Implementing Agency

(i) Develop a state-of-the-art facility for training faculty and providing trained manpower to the ICTE industry.

(ii) Develop and maintain a world class curriculum related to the ICTE industry, with inputs from both industry and academia.

(iii) Offer specialized training to the faculty in the Engineering, Arts, Commerce & Science Colleges and Polytechnics across the State/UT.

(iv) Offer research orientation to faculty.

(v) Carry out research and consultancy support for industry for capacity building and courses in ICTE areas.

(vi) Function as a Resource Centre for curriculum and faculty development for mass based HR programmes in the respective region.

(vii) Offer training to faculty and students in other emerging areas in ICTE. A close association with industry shall be maintained by the Academy so as to capture the new emerging requirements and ensure timely interventions.

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(viii) Each Academy would launch a set of training programmes and other activities to become self-sustainable. The activities could include Instruction Enhancement Programme (IEP) for faculty, Continuing Engineering Education Programme for working professionals, Joint Industry Attachment Programme for students, enhancing the quality of institutions by guiding them to obtain ISO standards, etc.

(ix) Each Academy would create a suitable mechanism for identification of the beneficiary and the linkage of beneficiary identification with UID numbers, wherever available or other suitable mechanism. Further, an appropriate Management Information System (MIS) would be created to register the details of beneficiaries, types of courses and other appropriate details.

(x) Each Academy would set-up an **Academic Committee** and a **Research Committee** with relevant experts from industry, Sector Skill Councils and academia which would recommend various courses/training programmes proposed to be launched by the respective Academy. While the Research Committee would advise on the emerging areas on which the faculty development could be initiated, the Academic Committee would take care of various aspects like development of new courses, syllabus, course content, curriculum, e-content, identification of experts, etc. This is to ensure that the training programmes are as per the emerging requirement in the electronics and ICT sector and also in line with the local/region specific requirements.

(xi) The quality, standard of the courses and other activities of each Academy would be required to be maintained through Academic and Research committees. These committees may also have representation from similar committees set up by other Academies to facilitate learning from each other, cross-fertilisation of ideas and standardisation of various courses and course content etc.

(The details are at Annexure-I)

6. FINANCIAL DETAILS:

6.1 The Budget outlay of the Scheme for Financial Assistance for setting up of Electronics and ICT Academies for each category is depicted below. The Budget Outlay for each Implementing Agency is at **Annexure-II**.

(Rs. in Crore)

S. No.	Head	Category A	Category B
A	Total Outlay	25.00	10.00
B	Revenue Generation (Estimated)	7.50	3.00
C	Grant-in-Aid support from DeitY for four (04) years (A – B)	17.50	7.00

6.2 The relevant details are as per Administrative Approval No. 3(6)/2012-HRD (Vol. III) dated 14.11.2014 as amended from time to time.

6.3 The Grants-in-Aid will be regulated in accordance with the provisions contained in Chapter 9 of the General Financial Rules, 2005, as amended from time to time, read with the Government of India's decisions incorporated there-under, and any other guidelines which may be issued in this regard. Implementing Agency would also be governed by the standard Terms & Conditions of Grants-in-Aid of DeitY **(Annexure-III)**. All financial transactions will be subject to the requirements of the *Fiscal responsibility & Budget Management Act*.

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6.4 The detailed guidelines on common operational and functional framework for all the Academies would be issued by DeitY subsequently. Each selected institution/Academy would need to abide by the financial aspects as per these guidelines.

7. APPOINTMENT OF CHIEF INVESTIGATOR & CO-CHIEF INVESTIGATOR

To ensure the successful implementation of the Project, Implementing Agency will appoint a Chief Investigator and a Co-Chief Investigator for the Project. The Chief Investigator will have the overall responsibility of the implementation of the Project. During the period the Chief Investigator is not available, the Co-Chief Investigator will perform the duties of the Chief Investigator. **The Chief and Co- Chief Investigator of the Project will not be changed as far as possible during the course of the Project.**

8. DURATION OF THE PROJECT

The scheme duration is five years w.e.f. 14.11.2014. Project duration of each Academy would be for a period of four (04) years from the date of approval. Any need for its extension, if essential, will be reviewed by the Project Review & Steering Group (PRSG) for its further consideration and approval by DeitY. However, it would be the endeavor of both parties to this MOU to complete the Project within the stipulated period. DeitY will not bear any expenditure towards recurring, upgradation or maintenance expenses after the completion of the Project.

9. COMPLETION OF PROJECT

The Project shall be deemed to have been successfully completed when Implementing Agency achieves the desired objectives of the Project as brought out in this MOU. Implementing Agency will submit a Project Completion Report within one month of the completion of the project.

10. INTELLECTUAL PROPERTY RIGHTS (IPR's)

10.1 Implementing Agency shall make all efforts to protect Intellectual Property generated out of the Project. They will first examine IPR protection issues in consultation with IPR Cell, DeitY to file patents, register copyrights, designs, trademarks etc., before making it public by publishing in the technical journals and books, presenting findings in conferences etc.

10.2 Intellectual Property and the rights associated with it shall be assigned jointly to DeitY and Implementing Agency. In cases where funding has been done jointly with other organisations, the IP Rights would be appropriately shared.

11. CONFIDENTIALITY

Implementing Agency undertakes on its behalf and on behalf of its subcontractors/ employees to maintain strict confidentiality of the Project including, but without limitation to, the R&D work and know-how generated and prevent, disclosure thereof, for any purpose, other than in accordance with this MOU. DeitY, in turn, will also

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ensure confidentiality as required for the Project. The provisions of this clause will outlive this MOU.

12. UTILIZATION OF TECHNOLOGY GENERATED UNDER THE PROJECT

Implementing Agency will have the right to distribute Awareness Material, Learning Material developed or other IPR's generated through the project for use by others. However, this arrangement is subject to the terms and conditions of grant-in-aid prescribed by DeitY. Implementing Agency will also inform DeitY about such an arrangement.

13. FORCE MAJEURE

Neither party shall be held responsible for non-fulfillment of their respective obligations under this MOU due to the exigency of one or more of the force majeure events such as, but not limited to, Acts of God, war, flood, earthquakes, strike, lockouts, epidemics, riots, civil commotion etc., provided on the occurrence and in cessation of any such event, the party affected thereby shall give a notice in writing to the other party immediately after but not later than one month of such occurrence and cessation. The period between the occurrence and cessation of such event will be excluded while calculating the period during which the party has to perform his obligations under this MOU. If the force majeure conditions continue beyond six months, the parties shall then mutually decide about the future course of action.

14. TERMINATION OF THE PROJECT

(i) DeitY will have the right to terminate the MOU based on recommendation of the PRSG at any stage, if it is satisfied that:
   (a) the money released has not been properly utilized, or
   (b) appropriate progress on the Project is not being made, or
   (c) the Project is not being carried out as per the terms and conditions and/ or as per the nature and scope of work as defined in the approved Project proposal.

(ii) If Implementing Agency faces difficulties in implementing the Project for any techno economic and reasons other than the above, based on the recommendations of the PRSG and as directed by DeitY, Implementing Agency shall pay back all unspent DeitY grants released and Hardware & Software supplied for the Project and interest accrued thereon and/or any amounts recoverable by way of disposal of assets procured out of DeitY funds.

(iii) If Implementing Agency abandons the Project on their own without approval of DeitY, then DeitY will have the right to recover from Implementing Agency the money disbursed and Hardware/Software procured for the Project along with 12% simple interest.

15. SAVING PROVISIONS

Implementing Agency agrees to disclose and provide DeitY or its authorized representative or agency, such disclosure, the know-how, the related process and the intellectual property rights to use and practice the same for the purpose of experimentation and/or further research or development thereof, with the right to manufacture, sell and vend the "Products" in such a manner as Government of India may, in its judgment decide, for "Government purposes", or otherwise in public

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interest. DeitY may compensate Implementing Agency for such commercial exploitation of the know-how, process and related IPR. Decision of Secretary, DeitY in regard to such compensation shall be final.

16. VALIDITY

16.1 The duration of this MOU will be for a period of four years w.e.f. date of Administrative Approval or till completion of the Project, whichever is later.

16.2 Any matter not covered specifically in the MOU may be settled by mutual agreement. On points of disagreement, the matter may be referred to Secretary, DeitY for a decision, which shall be final and binding on both the parties.

17. MODIFICATIONS TO THE MEMORANDUM OF UNDERSTANDING

The MOU can be modified through mutual written consent of all the parties to this MOU.

18. SEAL OF PARTIES

In witness whereof the parties hereto have signed this MEMORANDUM OF UNDESTANDING on the day, month and year mentioned herein before.

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[For and on behalf of the President of India]
Department of Electronics and Information Technology
Ministry of Communications and Information Technology
Government of India
Electronics Niketan
6, CGO Complex
New Delhi – 110003.

.....

[For and on behalf of Implementing Agency]
(I. K. BHAT) Director
Director
Malaviya National Institute of Technology Jaipur
JAIPUR-302017 (Rajasthan)

.....

.....

IN THE PRESENCE OF WITNESSES

Signature:	.....	Signature:	.....
Name:	.....	Name:	Akhadhesh Bhardwaj
Occupation:	.....	Occupation:	Teaching Dean(R&C)
Address:	.....	Address:	M.N.I.T. Jaipur
	.....		.....
	.....		.....
	.....		.....

(V. SAHULA)
PROF, ECE & CI

(LAVA BHARGAVA)
MNIT

LIST OF ANNEXURES

Annexure-I

General description / Salient features of Electronics & ICT Academy:

- Electronics and ICT Academy would be set up as a unit under the respective institution with the financial assistance of the Central Government for four years.
- Each Academy would ensure the following:
  a) Entry/Exit criteria for 'trainees'
  b) Adoption of at least 10% Computer Based Training(CBT) modules
  c) Observance of rules of reservation for SC/ST candidates as per Government of India policy
  d) At least 25% of trainees to be from Electronics streams.
- Each Electronics and ICT Academy would aim to provide specialized training to the faculties of the Engineering colleges in the emerging areas of electronics & ICT; and training large number of faculties from Arts, Commerce & Science colleges, Polytechnics, etc in the areas of utilisation of IT tools and techniques for application in their respective domain of knowledge/learning/teaching/enhancing productivity, etc by developing state-of-the-art facilities.
- Each Electronics and ICT Academy would focus on improving the quality of faculty of institutes and colleges in the respective states/UTs which would result in improvement of quality of students there by making them industry ready and employable in the ICT/ Electronics Manufacturing Industry.
- Each Electronics and ICT Academy would offer identified training programmes to faculty members on contemporary industry related subject areas where there is industry demand but shortage of skills.
- The main thrust is to facilitate faculty to be abreast with the latest developments in technology and emerging industry needs.
- Research orientation especially to the engineering faculty of Electronics and IT and related streams would be emphasised by integrating it with the training programmes. A one/two day Workshop/Seminar on latest technological trends and possible research topics that can be taken up in these areas would be included in each training programme.
- The trained faculties are expected to train students in various institutes. This is expected to have a cascading effect and the benefit is expected to reach the large number of students in the respective states.
- In addition, each Electronics and ICT Academy could also provide focused training to select/ limited nos. of students in order to maximizing the utility of the infrastructure/facilities created in the academy. Further this would provide a platform for learning from the students training to readjust/redesign the faculty training/program.
- Each Electronics and ICT Academy would conduct standard training programmes that would address the basic needs of the ICTE industry. The Academy would also conduct specialized programmes based on specific industry needs from time to time. The training will extensively use latest internet and communication technology infrastructure. The course would be revised as per the latest industry trends in every three years.
- The Academies would be setup in two categories i.e. Category A and B. The target of Faculty Members to be trained in each of these Categories in 4 years are as under:

Category	No. of Academies	Target for 4 years by each Academy	Total target
Category A	05	16,000 candidates	80,000 candidates
Category B	02	6,400 candidates	12,800 candidates
Total target in four years by 07 Academies			**92,800 candidates**

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- Each Academy would focus on at least one newly emerging areas in Electronics (e.g. Automotive electronics, LEDs, Industrial Electronics, Medical Electronics, Telecom, Avionics, Displays, Rechargeable Batteries, Solar, Railways, I&B, Games) or IT (e.g. Localization, Virtualization, Cloud Computing, Next Generation Computing Systems, High Performance Computing (HPC), GIS, Mobile Technologies, Inter-operable Infrastructure for Small Financial Transactions, Switch, Language Technologies, etc.).
- Each Electronics and ICT Academy would be provided with a funding support for refurbishment of existing premises and purchase of equipment for setting up the state-of-art labs; support for Skilling/training cost per faculty being trained; Project Management Unit & MIS. Average training cost per candidate is estimated as Rs.12,500/- per candidate depending on the total target assigned. The average training duration is envisaged to be 2-weeks full-time [equivalent to a 3-credit course of about 45-48 hrs duration with additional provision of lab/hands-on component and a one/two day Workshop/Seminar on latest technological trends and possible research topics that can be taken up in these areas]. This cost could vary depending on the type of course and duration based on the level of faculty being targeted. However, the ratio of total skilling/training cost vs. the targets shall remain the same for the purpose of arriving at the total outlay and funding support requirement.
- Each Academy would aim to generate revenue by charging fee and taking up other activities from the second year onwards to meet the remaining cost in a gradual manner and become self-sustainable by the end of fourth year onwards.
- An indicative List of Courses and Course Structure for Faculty Training Programs are given at **Appendix to Annexure-I**.

- **Sustainability**

  Each Academy is expected to generate revenue by charging fee and taking up other activities from the second year onwards to meet the remaining cost in a gradual manner and become self-sustainable by the end of fourth year onwards. No funding support from the Central Government is envisaged after the completion of four year project duration in respect of each Academy. A steady revenue stream as continuous source of income generating activities of the Electronics and ICT Academy is expected from design and development of various kinds of courses aimed faculty, students, working professionals, conducting training both through direct mode as well as through on-line courses, provide Research & Development and other consultancy as well as capacity building and training services in the emerging cutting edge technologies. The activities could include Instruction Enhancement Programme (IEP) for faculty, Continuing Engineering Education Programme for working professionals, joint Industry Attachment Programme for students, enhancing the quality of institutions by guiding them to obtain ISO standards, etc. Other indicative set of activities that are envisaged to be taken by each Academy to achieve self-sustainability are given below:

  - **Industrial Services**: Technology Extension Service to Industry
    - **Corporate Training Activity:** The major source of income of the Academy is expected to be from specialized tailor made courses designed with academic inputs as per requirements of the industry both for the fresh recruits as well as for up-gradation of their other employees in the emerging areas to improve the productivity.
      - Fresh Recruits – Specially designed courses for bridging the gap between industry requirements and knowledge and skill gained through formal education.
      - Skill/knowledge upgration courses for the working professionals

- **R&D and other Consultancy services:**
  - Undertaking collaborative result oriented projects / technology or development of products jointly in the emerging areas
  - Identifying and sharing best practices
  - Provide guidance for creation of advance facility to undertake R&D
  - Provide technical support for small and medium scale industries
  - Resource sharing by way of HRD Training, Consultancy for industry services and collaboration
  - Provide technical support and expertise for selection of technology and its absorption / adoption
  - Capability development for indigenous technology / products
  - Solution development / product design work for the industry

- **Awareness and orientation programmes-**
  - Creation of awareness about emerging/ upcoming and cutting edge technologies and motivate / encourage them to implement these for increasing yield of quality products
  - Also create awareness in emerging fields having social impact such as Electronic Waste Management, Green IT, Ubiquitous computing, eco-friendly design and technology for differently abled people etc.
  - Design, development and implementation of appropriate and affordable technology for the use of masses, particularly targeting applications required for rural areas.

- Further, the Academies could also train the students directly on chargeable basis for making them industry ready or to become self-employable. The Academies could target capability development for indigenous technology / products, value added employment oriented courses, entrepreneurial development programmes, Skill development / knowledge upgradation courses, etc. for Working professionals/Self Employed entrepreneurs, etc.

- Thus, each Academy would, apart from meeting the ongoing need to train faculty and students, would also develop specialized training programmes to meet the specialized sector-specific needs of the IT/ITeS, BPO, Electronics Hardware and Manufacturing companies which would help it to become self-sustaining. In addition to the educational programmes, the Academies are also expected to build internal capacities to take up industrial consultancy; sponsored research projects for both government and industry; solution development / product design work for the industry; and also provide focused industry specific training programs etc. to generate substantial revenues for making it self-sustainable.

Note : The detailed guidelines on common operational and functional framework for all the Academies would be issued by DeitY subsequently. Each selected institution/Academy would need to abide by these guidelines (including financial aspects).

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Appendix to Annexure- I

Indicative List of Courses and Course Structure for Faculty Training Programs

A. **Indicative list of courses for IT and non-IT faculty members**

1. IT courses for Engineering faculty members of Electronics and Computer Science
   - Brushing up of fundamentals of relevant engineering subjects
   - Industry need based advance courses such as- J2EE & BPAD, Essentials of .Net and C#; Digital Signal Processing System Design; C#, Applied Microsoft .NET Framework Programming; Java Programming, .Net Programming ; Intel Multi-Core Programming ; MATLAB Fundamentals and Image Processing Toolbox ; Cloud Computing ; RF Wireless Communication System Design ; Embedded System Design ; VLSI Signal Processing
   - Research Orientation in the area of electronics and computer science on topics of current research interests and emerging research issues, emerging technologies and market orientation (in a two weeks program one day would be devoted for addressing these aspects)
   - Soft skills (optional) as - Behavioral Skills, Time & stress management, relaxation techniques, Communication Skills, Corporate Culture & Professional ethics, Time Management, Presentation & Interview skills: Reducing stress with effective planning, Conversation & Group Discussions etc.

2. IT courses for Engineering faculty members other then Electronics and Computer Science viz. mechanical, chemicals, civil, aeronautical etc.
   - Fundamentals of Computers, Operating System, ICT Tools and Techniques and its applications to their respective fields, etc. ;
   - Research Orientation with reference to emerging IT technologies which have direct impact on various applications in other engineering domains, which could lead to enhancement of productivity, application of newer and novel solutions and changing market trends, etc.
   - Soft skills (optional): As mentioned above

3. IT courses for Arts faculty members
   - Brushing up of fundamentals about knowing and operating computers, introduction to Information Security, etc.
   - Use/application of IT or say application of IT in arts domain – Photoshop, photography, photo editing, video-editing, MP4, audio-editing, MP3, DTP, Graphics, digitization/ scanning, website design, e-book, designing of logos etc.
   - Sessions on emerging technologies and their application to various Arts subjects
   - Soft skills(optional): As mentioned above

4. IT courses for Commerce faculty members
   - Brushing up of fundamentals about knowing and operating computers, introduction to Information Security, etc.
   - Use of IT application in commerce domain - Tally, banking/accounting software, commercial portals/websites for products and services, individual business software for management etc.
   - Sessions on emerging technologies and their application to various Commerce subjects
   - Soft skills (optional): As mentioned above

5. IT courses for Science faculty members
   - Brushing up of fundamentals about knowing and operating computers, introduction to Information Security, etc.
   - Use of IT applications in science domain - Animation based learning, models, experiments, analyzing tools, accesses/sharing of e-sources, database, research papers, e-books, research & education websites/portals etc.
   - Sessions on emerging technologies and their application to various Science subjects
   - Soft skills (optional): As mentioned at Para 1.4 above

6. IT courses for Polytechnic faculty members of Electronics & Computer Science
   - Basics and fundamentals of core engineering subjects - Programming languages, Java Programming, .Net Programming etc.
   - Sessions on emerging technologies and their applications to various subjects.
   - Soft skills (optional): As mentioned above

7. IT courses for Polytechnic faculty members other than Electronics and Computer Science.
   - Brushing up of fundamentals about knowing and operating computers, introduction to Information Security, etc.
   - Sessions on emerging technologies and their application to various subjects.
   - Soft skills(optional): As mentioned above

B. **The Indicative List of Advanced Training Programs and Course Structure for Electronics and Computer Science Faculty members**

Some of the topics and the syllabus of Advanced Faculty Training programs for these areas are given below:

1. **Hands-on With ARM: Programming Embedded Systems**
   - ARM Architecture and Organization ; ARM Assembly Programming ; THUMB Assembly Programming ; ARM-THUMB Interworking ; Assembly and C Mixed Programming ; Exception Handling ; ARM Toolchain (Assemblers, Compilers, Linkers & Debuggers) ; Firmware Programming ; Caches & MMU ; Peripheral Programming ; ARM Cortex family of processors and architecture ; Operating modes, Registers and Memory Map of Cortex-M3 ; Embedded OS ; Porting of Embedded OS on ARM

   Pre-requisites
   - Basic Knowledge in Microprocessors / Micro controllers, C Programming

2. **Security Engineering**
   - Introduction to Security Engineering ; Overview (Attacks, Mechanisms and Services); Goals of Security (Detection, Prevention and Recovery) ; Network Packet Capturing and Analysis ; Introduction to Cryptography & Types of Cryptographic Algorithms ; Hash Functions & Digital Signatures ; PKI and Digital Certificates ; Authentication & Access Control ; e-Mail Security, Web Security with TLS/SSL ; Perimeter Security Solutions (Firewall, IDS and VPN) ; IP Security, Database Security ; Information Security Standards, Security Design Principles ; Security Architectures and Models ; Secure Coding Practices in C & C++ ; Security Testing and Evaluation Criteria

   Pre-requisites
   - Sound knowledge in operating system concepts, networking and C programming

3. **Mobile Application Development**
   - Overview of Mobile Platforms: JavaME and Android ; Introduction to Mobile Application Development ; Sockets and Bluetooth Programming on Mobile ; Mobile Databases ; Mobile Enterprise Application Development ; Secure Mobile Application Development

   Pre-requisites
   - Basics of Core Java, Networking etc.

4. **Enterprise Solutions for Web Applications**
   - Introduction to Web programming ; JDBC ; Servlets, JSP and JSTL ; Hibernate ; Introduction to JEE frameworks ; Mini project based on above topics

   Pre-requisites
   - Core java, Fundamentals of database technologies, Basics of web programming (HTML, Java script)

5. **Linux System and Multicore Programming**
   - Introduction to Linux System Programming ; Shell, Environment & Linux Architecture ; GNU Tool Chain (GCC, GDB, MAKE, GPROF & GCONV) ; System Calls and Working with Files ; Process Management & IPC ; Socket Programming ; Parallel Programming Paradigms ; MultiCore Architectures ;Modeling Performance - Amdahl's Law, Gustafson's Law ; System Overview of Threads ; Threading and Parallel Programming Constructs ; Multithreaded Environment, POSIX threading APIs ; Data Races, Deadlocks, and Live Locks ; Thread-safe Functions and Libraries ; OpenMP programs on multicore ; Message Passing Interface (MPI) Programming ; Performance Analysis of multithreaded programs ; Multithreaded Debugging Techniques ; High Performance Computing – Cluster, Grid

   Pre-requisites
   - Sound knowledge in operating system concepts, networking and C programming

6. **Network Programming and Security Engineering**
   - Introduction to Security Engineering, Attacks, Mechanisms and Services, Attack Detection, Prevention and Recovery ; Network Packet Capturing and Analysis ; Authentication and access control, email security and web security ; Perimeter Security Solutions – IDS, Gateway Firewall and VPN ; Introduction to Malware and Analysis ; Security Standards and Auditing ; Client-Server Paradigm, TCP & UDP based network programming ; Multithreaded servers with I/O multiplexing and Synchronization ; PCAP programming, Security protocol implementation using Crypt library ; OpenSSL programming ; Secure coding in C & C++
     Secure coding in Java ; Web based threats and securing web applications ; Database Security ; Security design principles, architectures & models ; Security Testing and Evaluation Criteria

   Pre-requisites
   - C / C++ Programming, Data Structures, OOPs concepts, Networking & TCP/IP Concepts, OS Concepts, Working knowledge of Linux & Windows OS, Internet & Web Concepts

7. **Network Security and Malware Analysis**
   - Introduction to Security Engineering, Attacks, Mechanisms and Services, Attack Detection, Prevention and Recovery ; Network Packet Capturing and Analysis ; Authentication and access control, email security and web security ; Perimeter Security Solutions – IDS, Gateway Firewall and VPN ; Database Security ; Security

Standards and Auditing ; Introduction to Windows Architecture ; Windows Programming and API, PE format

Windows Security Concepts ; Data Structures in Windows and Kernel Programming ; Introduction to Malware, Automated Analysis, Behaviour Analysis ; Malware Analysis with samples ; Dealing with Advanced Malware ; Analysing Memory Images with Volatility Toolkit ; Analysing Web based malware, malicious documents; Analysing vulnerability exploitation which is carried out using Metasploit Framework

Pre-requisites

- C / C++ Programming, Data Structures, Networking & TCP/IP Concepts, OS Concepts, Working knowledge of Linux & Windows OS

8. **System Design using FPGA**
   - VLSI Design Flow ; FPGA Architecture ; Hardware Description Language ; Designing and Implementation of Finite state Machines for FPGA ; Synthesis Techniques and Timing Analysis ; Placement and Routing ; Embedded Hardware and Software Design with FPGA ; Porting Embedded Operating Systems on FPGA ; Case Study on FPGA based System Design

   Pre-requisites
   - C, Microprocessors, Microcontrollers, Digital Electronics, Knowledge in computer science, Basic concepts in VLSI

9. **Parallel Programming for Scientists and Engineers**
   - Advanced Computer Architectures ; Introduction to Parallel Programming ; Principles of Parallel Algorithm Design ; Building Compute Clusters ; Numerical Computing ; Programming Paradigms ; OpenMP ; Message Passing Interface (MPI) ; Advanced MPI ; Performance Analysis and Debugging Parallel Programs ; Parallel Applications/Case Studies ; GPGPU & CUDA programming ; Grid Computing ; Cloud Computing

   Pre-requisite
   - C/C++ with Data Structures, familiarity with Linux / Unix

10. **Hardware and Firmware design for ARM based Embedded Systems**
    - Overview of 32 bit Microcontrollers ; Microcontroller based Hardware Board Design ; Kit fabrication and testing ; Cortex M3 overview and Basics ; Instruction Set and Memory Subsystem ; Programming and debugging in Eclipse ; Exceptions and Interrupt Handling ; Programming Stellris Cortex ; Kit Interfacing and Programming - Switches, LEDs, Temperature/Light Sensors, PS2 keyboard, VGA display Audio Sampling, Embedded RTOS ; RTOS Drivers ; Porting of Embedded RTOS on ARM ; JTAG Debugging and Case Studies ; Power Saving modes ; Variants of ARM boards ; Mini project

    Pre-requisites
    - C, Microprocessors, Microcontrollers, Digital Electronics

11. **Electronic Manufacturing and Product Design**

    a) **Electronics (PWB) Design & Manufacturing :** Design rules for Analog, Digital, Power circuits & high frequency circuits ; PCB design using CAD packages ;Electronics Manufacturing of SSB, DSB, MLB ; Trends in Electronic Design and Manufacturing ; Wire Harness

    b) **Product Design** : Product design in Product development ; Product Design Methodology ; Elements of Aesthetics ; Layout design, structure design ; Product detailing is sheet metal and plastics for case of assembly, maintenance and aesthetics ;

Thermal design of Electronics equipments and case studies ; Product Manufacturing ; Value Engineering ; Physical Design of Electronics Equipment set

c) **Mechanical Design** : Physical Design in product Development Process using as - Computer Aided Design (CAD Software) ; Solid Modeling ; 3D Manipulation ; Digital Imaging

12. **FPGA based system Design : A SOC approach**
    - FPGA Architecture ; FPGA Tool Chain Flow ; SoC Architectures ; RTOS Flavors for SoCs ; Advanced memory: DDR, DDR2, DDr3, QDR SRAM ; Memory Controllers for SoC architecture ; Functioning of Coprocessors in SOC ; Cache/MMU in SoC – functioning of Cache Controller ; Low Speed Interfaces : UART, SPI, I2C ; High Speed Interfaces : Ethernet, USB, PCI ; Implementation of System building blocks using VHDL ; Analog System Design ; Hands-on Lab: using FPGA lab kits and Analog Lab kits

    Pre-requisite
    - Digital Design experience, VHDL programming

13. **Information Security on VTE**
    - Information Gathering & Countermeasures
    - Network Discovery & Scanning ; Target Enumeration ; Vulnerability Assessment
    - Ethical Hacking & Countermeasures
    - Sniffing & Countermeasures ; Brute Force Attack & Countermeasures ; IP Spoofing with DOS & Countermeasures ; Trojan, Backdoor, Virus & Countermeasures ; Bypassing Proxy & Countermeasures ; SQL Injection Attack & Countermeasures ; Code Injection & Countermeasures ; E-mail Spoofing, Phishing & Countermeasures ; Hacking Wireless Network & Countermeasures
    - Hardening, Perimeter Security & Evaluating Security
    - E-mail Security ; Network Traffic Analysis ; Network Traffic Encryption ; Installing & Configuring Intrusion Detection system ; Configuring Host Based Firewall ; Host System Hardening (Windows) ; Host System Hardening (Linux) ; Evaluating Security
    - Advanced Penetration Testing techniques
    - Python Basics, Security testing on various network Protocols: HSRP, VRRP, SMTP, CDP etc.
    - Linux Exploitation
    - Windows Exploitation
    - Reverse Engineering Techniques

14. **Intelligent Transportation System**
    - Introduction to ITS, ITS architecture & Toolkit ; Vehicle tracking system & Sensing methods ; VMS & RFID systems ; Train information system ; Distress call management system ; Automated tolling system ; Mathematical tools for ITS ; Traffic flow modeling, Traffic controllers – evolution ; Fixed, Vehicle actuated Traffic controllers (UTCS) ; ATCS – CoSiCoSt ; Products developed under ITS programme by DeitY ; Wireless traffic controller - Design and Demo, Counting and classification ; Intelligent transit trip planner and real time route information ; Parking Management System - Design and Demo ; Advanced Traveler Information ; Red light violation detection - Design and Demo ; Speed violation detection ; Collision avoidance / notification system ; Bus Priority System (BRT / Preemption) ; WAVE Communication

15. **Digital Signal Processing and Image Processing**

- Introduction to Digital Signal Processing ; Frequency Domain Analysis ; Image Processing Basic algorithms and applications ; Speech Processing Basic algorithms and applications ; Pattern Recognition ; Soft Computing Techniques ; Case Studies ; Embedded Signal Processing

16. **VLSI and Embedded Systems**

- **Module 1: System Design using FPGA**
  VLSI Design Flow ; FPGA Architecture ; Hardware Description Language ; Designing and Implementation of Finite state Machines for FPGA ; Synthesis Techniques and Timing Analysis ; Placement and Routing ; Embedded Hardware and Software Design with FPGA ; Porting Embedded Operating Systems on FPGA ; Case Study on FPGA based System Design ; SOC design Flow
- **Module 2: Embedded Systems Design**
  Overview of 32 bit Microcontrollers ; Microcontroller based Hardware Board Design; Instruction Set and Memory Subsystem ; Programming of Interfacing Modules ; Implementation of digital filters on DSP Processor ; RTOS and device Driver

Note:

1) All the above programs should have suitable Lab emphasis and Research Focus/ Orientation
2) The above courses are indicative purpose and could be used as reference.

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Annexure- II

Table 1: Budget Outlay per Category A Institution

(Rs. in Crore)

S. No.	Head	Year-1	Year-2	Year-3	Year-4	Year-5	Total
A	**Capital**						
(a)	Refurbishment of existing premises & other infrastructure	1.50	0.00	0.00	0.00	0.00	1.50
(b)	Equipment (H/W & S/W)	2.50	0.00	0.00	0.00	0.00	2.50
	Sub Total (A)	4.00	0.00	0.00	0.00	0.00	4.00
B	**Recurring expenses**						
(a)	Skilling cost	5.00	5.00	5.00	5.00	0.00	20.00
(b)	Project Management Unit & MIS	0.25	0.25	0.25	0.25	0.00	1.00
	Sub Total (A)	5.25	5.25	5.25	5.25	0.00	21.00
C	**Total Outlay (A + B)**	**9.25**	**5.25**	**5.25**	**5.25**	**0.00**	**25.00**
D	**Revenue Generation**	**0.00**	**1.25**	**2.50**	**3.75**	**0.00**	**7.50**
E	**Grants-in-Aid (C - D)**	**9.25**	**4.00**	**2.75**	**1.50**	**0.00**	**17.50**

Contribution of Stakeholders

- Central Govt. : Rs. 17.50 crore
- State / UT Administration : Nil
- Identified Implementing Agencies : Land, building, other infrastructure and all other resources required to set up the Academy
- Revenue Generation (Estimated) : Rs. 7.50 crore

Table 2: Budget Outlay per Category B Institution

(Rs. in Crore)

S. No.	Head	Year-1	Year-2	Year-3	Year-4	Year-5	Total
A	**Capital**						
(a)	Refurbishment of existing premises & other infrastructure	0.75	0.00	0.00	0.00	0.00	0.75
(b)	Equipment (H/W & S/W)	0.75	0.00	0.00	0.00	0.00	0.75
	Sub Total (A)	1.50	0.00	0.00	0.00	0.00	1.50
B	**Recurring expenses**						
(a)	Skilling cost	2.00	2.00	2.00	2.00	0.00	8.00
(b)	Project Management Unit & MIS	0.20	0.10	0.10	0.10	0.00	0.50
	Sub Total (B)	2.20	2.10	2.10	2.10	0.00	8.50
C	**Total Outlay (A + B)**	**3.70**	**2.10**	**2.10**	**2.10**	**0.00**	**10.00**
D	**Revenue Generation**	**0.00**	**0.50**	**1.00**	**1.50**	**0.00**	**3.00**
E	**Grants-in-Aid (C - D)**	**3.70**	**1.60**	**1.10**	**0.60**	**0.00**	**7.00**

Contribution of Stakeholders

- Central Govt. : Rs. 7.00 crore
- State / UT Administration : Nil
- Identified Implementing Agencies : Land, building, other infrastructure and all other resources required to set up the Academy
- Revenue Generation (Estimated) : Rs. 3.00 crore

Note:

a) The financial support from DeitY would be 100% in first year, 75% in second year, 50% in third year and 25% in fourth year. Each Academy is expected to generate revenue by charging fee and taking up other activities from the second year onwards to meet the remaining cost in a gradual manner and become self-sustainable by the end of fourth year onwards. No funding support from the Central Government is envisaged after the completion of four year project duration in respect of each Academy.

b) Average training cost per candidate is estimated as Rs.12,500/- per candidate depending on the total target assigned. The average training duration is envisaged to be 2-weeks full-time [equivalent to a 3-credit course of about 45-48 hrs duration with additional provision of lab/hands-on component and a one/two day Workshop/Seminar on latest technological trends and possible research topics that can be taken up in these areas]. This cost could vary depending on the type of course and duration based on the level of faculty being targeted. However, the ratio of total skilling/training cost vs. the targets shall remain the same.

c) The detailed guidelines on common operational and functional framework for all the Academies would be issued by DeitY subsequently. Each selected institution/Academy would need to abide by the financial aspects as per these guidelines.

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ANNEXURE-III

TERMS AND CONDITIONS GOVERNING GRANT-IN-AID

i) The grant is for the specific project as approved by the Department of Electronics and Information Technology (DeitY) and shall be subject to the following conditions:

a) The grant amount shall be spent for the project within the specified time
b) Any portion of the grant, which is not ultimately required for expenditure for the approved purposes, shall be duly surrendered to DeitY.

ii) The grantee institution shall maintain an audited record in the form of a register in the prescribed proforma for permanent, semi-permanent assets acquired solely or mainly out of DeitY grant;

iii) The assets referred to in (ii) above will be property of DeitY and should not, without prior sanction of DeitY, be disposed off or encumbered or utilised for the purposes other than those for which the grant has been sanctioned. An undertaking shall be given by the grantee institution that they agree to be governed by these conditions;

iv) At the conclusion of the project, DeitY will be free to sell or otherwise dispose of the assets which are the property of DeitY and grantee institution shall render to DeitY the necessary facilities for facilitating the sale of these assets;

v) The grantee institution shall send to DeitY at the end of each financial year as well as at the time of seeking further installments of the grant a list of assets referred to in (ii) above;

vi) Should at any time grantee institution cease to exist, such assets etc., shall revert to DeitY;

vii) The grantee institution shall render progress-cum-achievement reports at interval of not exceeding six months on the progress made on all aspects of the project including expenditure incurred on various approved items during the period.

viii) The grantee institution shall render an audited statement of accounts to DeitY.

ix) The audited statement of accounts relating to grants given during financial year together with the comments of the auditor regarding the observance of the conditions governing the grant should be forwarded to DeitY within six months following the end of the relevant financial year;

x) The utilization of grant for the intended purposes will be looked into by the Auditor of grantee institution according to the directives issued by the Government of India at the instance of the Comptroller and Auditor General and the specific mention about it will be made in the audit report;

xi) DeitY or its nominee/s will have the right of access to the books and accounts of the grantee institution for which a reasonable prior notice would be given;

xii) The grantee institution should maintain separate audited account for the project. If it is found expedient to keep a part or whole of the grant in a bank account earning interest, the interest, thus earned should be reported to this Department. The interest so earned will be treated as a credit to the grantee to be adjusted towards future installments of the grant;

xiii) Sale proceeds of components, prototype, pilot project etc., fabricated as a result of the development of the project arising directly from funds granted by DeitY shall be remitted back to this department.

xiv) For the know-how generated by the project, guidelines for TOT/know-how transfer as given in Chapter VI of the *"Guidelines for Funding R&D Projects by DeitY"* will be applicable.

xv) DeitY will have the right to call for drawings, specifications and other data necessary to enable the transfer of know-how to other parties and the grantee shall supply all the needed data at the request of DeitY.

xvi) Application by grantee institution for any other financial assistance or receipt of grant/loan from any other Agency/Ministry/Department for this project should have the prior approval of DeitY.

xvii) The grantee institution is not allowed to entrust the implementation of this project for which grant-in-aid is received to another institution and to divert the grant-in-aid received from DeitY as assistance to the later institution.

xviii) DeitY shall appoint a Project Review and Steering Group (PRSG) comprising of representatives from DeitY and other experts. PRSG will periodically monitor the project in all respects including technical and financial.

xix) Grantee institution will examine IPR protection issues in consultation with IPR Cell, DeitY to file patents, register the copyrights etc. before making it public by publishing in the technical journals and books, presenting findings in Conferences etc.

xx) Institutions shall be encouraged to seek protection of Intellectual Property Rights (IPR) to the results of research through R&D Projects. While the patent may be taken in the name(s) of inventor(s), the institution shall ensue that the patent is assigned to it. The institution shall get its name entered in the Register of Patents as the proprietor of the patent. The Institution shall take necessary steps for commercial exploitation of the patent on exclusive/non-exclusive basis. The institution is permitted to retain the benefits and earnings arising out of the IPR. DeitY has a cell to guide and promote patent related matters (IPR cell).

xxi) In case of any dispute on any matter, related to the project during the course of its implementation, the decision of Secretary, DeitY, shall be final and binding on the institute.

xxii) In case the grantee institution is in receipt of more than fifty per cent of their recurring expenditure in the form of grants-in-aid, then the grantee institution should ordinarily formulate terms and conditions of service of their employees which are, by and large, not higher than those applicable to similar categories of

employees in Central Government and where it is not in accordance with the above, the relaxation of Ministry of Finance have been obtained as required under GFR 209(6)(iv)(a).

xxiii) The grantee institution agrees to make reservations for Scheduled Castes and Scheduled Tribes or OBC in the posts or services under its control on the lines indicated by Government of India.

xxiv) The accounts of the Grantee institution shall be audited by C&AG or by any person authorized by him on his behalf in accordance with the provisions laid down in Section 14 of the C&AG (DPC) Act, 1971 as amended from time to time.

xxv) The accounts of the grantee institution shall be open for inspection by the sanctioning authority and audit, both by the Comptroller & Auditor General of India under the provision of C&AG (DPC) Act, 1971 and internal audit party by the Principal Accounts Office of the Ministry or Department whenever it is called upon to do so.

xxvi) The grantee institution shall furnish certificate along with its request for release of Grants-in-Aid certifying that the fund released to them for which Utilization Certificate has not been issued, has been utilized exclusively in pursuance of object envisaged in their Rules/Memorandum and that the grant has been spent with the extent instruction/rules and with the approval of competent authority in each case.

xxvii) The grantee institution shall furnish a performance-cum-achievement report to the Sanctioning Authority before the release of the next installment of Grants-in-Aid.

xxviii) The grantee institution will spend Grants-in-Aid exclusively in pursuance of the objectives envisaged in their rules/memorandum and for the purpose it is being sanctioned.

xxix) Grants-in-Aid to the grantee institution is subject to the Economy Instructions issued from time to time by the M/o Finance or by the Competent Authority.

xxx) Grants-in-Aid shall be utilized before the end of the financial year and unspent balance, if any will be refunded by the grantee institution to the Govt. of India.

xxxi) Central Autonomous Organisations will maintain and present their annual accounts in the standard format, as required under GFR 209(6)(xiii).

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